CLAIMS

What is claimed is:

1. A method of designing an integrated circuit comprising programming a processing path within the integrated circuit according to a first substitute circuit comprising substitute inputs and a substitute output, wherein a truth table representing the first substitute circuit is identical to a truth table representing a first sequence of Boolean elements representing a processing path, and wherein the first substitute circuit is not definable by a sequence of basic Boolean circuits.

2. The method according to claim 1 further comprising generating the first substitute circuit.

3. The method according to claim 2 further comprising receiving the first sequence of basic Boolean elements.

4. The method according to claim 1 wherein the processing path further comprises a flip flop at a processing path input.

5. The method according to claim 2 further comprising the step of reducing the first sequence of Boolean elements into at least one intermediate equivalent circuit prior to the step of generating a first substitute circuit.

6. The method according to claim 2 wherein the integrated circuit is a MOS circuit.

7. The method according to claim 3 wherein the first sequence of basic Boolean elements is less than or equal to twenty Boolean operators.

8. The method according to claim 3 wherein the first sequence of basic Boolean elements comprises a logical sequence greater than twenty Boolean elements.

9. The method according to claim 3 wherein the step of receiving the first sequence of basic Boolean elements precedes the step of generating a first substitute circuit.

10. The method according to claim 1 wherein the step of programming is preceded by the steps:

a. generating a plurality of sequences of basic Boolean elements respectively defined by a plurality of truth tables;

b. generating a respective plurality of substitute circuits not definable by a sequence of basic Boolean elements, including the first substitute circuit, wherein a sequence of basic Boolean elements and its respective substitute circuit are defined by a same truth table;

c. storing the plurality of sequences of basic Boolean elements in a library; and

d. storing the plurality of substitute circuits in the library in a relationship corresponding to their respective sequence of basic Boolean elements.

11. The method according to claim 10 further comprising the steps:

e. receiving a first sequence of basic Boolean elements; and

f. searching the library for the first substitute circuit.

12. The method according to claim 11 further comprising the steps:

a. failing to locate the first sequence of basic Boolean elements within the library;

b. generating the first substitute circuit; and

c. adding the first substitute circuit to the library.

13. The method according to claim 11 wherein the step of receiving the first sequence of basic Boolean elements is followed by the steps:

a. locating the first sequence of Boolean elements within the library; and

b. locating the first substitute circuit within the library corresponding to the first sequence of Boolean elements.

14. The method according to claim 10 wherein the library comprises a digital memory.

15. The method according to claim 11 comprising a search engine for searching the library for the first sequence of basic Boolean elements.

16. An apparatus for reducing a throughput time of a processing path of basic logic elements within an integrated circuit, the apparatus comprising a programming module for programming a first substitute circuit into the processing path of the integrated circuit, wherein the substitute circuit is not defined by a sequence of basic Boolean circuits, and wherein the substitute circuit is defined by a truth table identical to a truth table defining a processing path comprised of basic Boolean circuits.

17. The apparatus according to claim 16 wherein the processing path comprises an input flip flop.

18. The apparatus according to claim 16 wherein the integrated circuit is an MOS circuit.

19. The apparatus according to claim 16 further comprising a circuit generation module configured to analyze a sequence of basic Boolean elements and generate a complimentary substitute circuit.

20. The apparatus according to claim 19 further comprising a reduction module configured to reduce a first sequence of Boolean elements into an intermediate circuit sequence.

21. The apparatus according to claim 16 further comprising:

a. a sequence generator for generating a plurality of sequences of Boolean elements, wherein the circuit generation module is configured to generate a complimentary substitute circuit for each sequence of Boolean elements generated;

b. a library for storing the plurality of sequences of Boolean elements such that each Boolean element is stored in a correlation to its complimentary substitute circuit;

c. a search module for searching the library for a first sequence of Boolean elements; and

d. a retrieval module for retrieving a substitute circuit from the library.

22. The apparatus according to claim 21 wherein the library is stored on a digital medium.

23. A method of programming a processing path comprising an input flip flop in a MOS integrated circuit comprises:

a. receiving a first sequence of basic Boolean elements;

b. reducing the first sequence of basic Boolean elements to an equivalent sequence of elements;

c. generating a substitute circuit from the equivalent sequence of elements; and

d. programming a processing path in the MOS integrated circuit according to the substitute circuit, wherein the substitute circuit is not definable by a sequence of basic Boolean elements, and wherein the substitute circuit is generated to define a truth table that also defines the first sequence of Boolean elements.